B1 cont'd such cells by reducing the integration interval and by controlling the electronic shutter to prevent the signal from reaching a saturation level.

The paragraph beginning on page 6, line 20, has been amended as follows:

The sensor cells in an array (as part of a sensor IC) may be monitored for saturation on a per column or row basis. The integration intervals may also be controlled on a per column or per row basis. If the sensor array is exposed to a scene having strongly lit areas, the photocells in a column or row detecting those areas will tend to saturate before the rest of the scene has been adequately detected. The B2 embodiments of the invention allow the row or column receiving strong light to be identified, its saturation to be prevented by ending integration for the affected row or column, and simultaneously continuing to integrate other rows or columns that received low light. This allows a more accurate image of the scene, closer to one obtainable from a perfect imaging system, to be captured in which both low and strong light areas are represented free of saturation effects and using a single exposure.

The paragraph beginning on page 7, line 17, has been amended as follows:

Figure 1 illustrates an embodiment of the invention as a sensor 100. The figure illustrates the photocell in terms of a circuit schematic featuring a BJT Q_1 that operates as a photodetector. In a particular embodiment, the photocell 100 is implemented using a standard logic complimentary MOS (CMOS) fabrication B3 cont process in which Q_1 is a PNP parasitic device built using a single n-well with highly doped p+ regions (such as implants) that may correspond to an unrealized MOSFET extending over portions of the n-well 204. Thus, Q_1 is realizable with a conventional CMOS process rather than a more expensive Bipolar-CMOS (Bi-CMOS). The p+ regions 208 and 212 are connected to electrical contacts that form the global emitter (GE) and pixel emitter (PE) contacts shown in **Figure 1**. A top view of Q_1 in this embodiment is illustrated in **Figure 2**, while **Figure 3** shows Q_1, being a parasitic PNP device, by way of cross section. It can be seen that the p-region 304